REMARKS

The Office Action dated June 21, 2001, has been received and reviewed.

Claims 1 through 6 and 8 through 24 are pending in the application.

Claim 7 has been canceled.

Claims 1 through 24 stand rejected.

Reconsideration of the above-referenced patent application is respectfully requested.

I. Drawings

Claim 7 has been canceled without prejudice or disclaimer, thus mooting this rejection.

II. Claim Objections

Claims 2, 9 and 19 were objected to due to informalities in the claim language. Appropriate correction has been made.

III. 35 U.S.C. § 112, First Paragraph

Claim 7 was rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 7 has been canceled without prejudice or disclaimer, thus mooting this rejection.

IV. 35 U.S.C. § 112, Second Paragraph

Claims 15-17 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

Specifically, the term "said carrier substrate" was found to lack antecedent basis. Claim 15 has been amended to remove the objectionable term "carrier", thereby ensuring that the term "substrate" has proper antecedent basis.

Therefore, it is respectfully requested that the 35 U.S.C. § 112, second paragraph, rejection of claims 15-17 be withdrawn.

V. 35 U.S.C. § 102(b) Anticipation Rejections

Claims 1-24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,786,628 to Beilstein, Jr. et al. (hereinafter "Beilstein").

Case law and the M.P.E.P. both hold that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Furthermore, the identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Beilstein teaches a multi-chip module in which stacked semiconductor devices 13 are vertically oriented relative to a connection structure 41. The bond pads (not shown) of each semiconductor device 13 of the multi-chip module disclosed in Beilstein are electrically connected to corresponding circuitry of the connection structure 41 by way of a series of conductive elements, including an elongate transfer metal structure 15 which contacts a corresponding, somewhat centrally located bond pad of a semiconductor device 13 and extends downward across a bottom edge thereof to an electrical contact 27 which, in turn, contacts a conductive bump 29 that is secured to a corresponding contact 53 of the connection structure 41.

Claim 1, as amended and presented herein, recites a semiconductor device that includes, among other things, a plurality of bond pads that are disposed adjacent an edge thereof and arranged substantially in-line. Amended claim 1 also recites that conductive bumps are disposed adjacent selected bond pads and that are configured to form conductive joints between a bond pad and a corresponding terminal of a substrate.

By way of contrast with amended claim 1, Beilstein is lacking of both express and inherent disclosure of a semiconductor device with bond pads disposed adjacent an edge thereof.

Rather, the elongate transfer metal disclosed in Beilstein infers that the bond pads are somewhat centrally located.

In addition, Beilstein does not expressly or inherently disclose conductive bumps that are disposed adjacent selected bond pads. Rather, in Beilstein, the conductive bumps are somewhat removed from the bond pads, with the transfer metal 15 and electrical contacts 27 being positioned between the bond pads of the semiconductor device 13 thereof and a corresponding contact 53 of the connection structure 41.

Furthermore, Beilstein includes no express or inherent disclosure of conductive bumps that are configured to form conductive joints between a bond pad of a semiconductor device and a corresponding terminal of a substrate. Rather, in Beilstein, the conductive bumps 29 merely form conductive joints between electrical contacts 27 on the bottom surface of the multi-chip module and corresponding contacts 53 of the connecting structure 41.

For these reasons, it is respectfully submitted that, under 35 U.S.C. § 102(b), amended claim 1 is allowable over Beilstein.

Claims 2-6 and 8 are each allowable, among other reasons, as depending either directly or indirectly form claim 1, which is allowable.

Claim 7 has been canceled without prejudice or disclaimer, rending the rejection thereof moot.

Independent claim 9, as amended and presented herein, recites a semiconductor device that includes, among other things, bond pads adjacent an edge thereof and arranged substantially in-line and conductive bumps adjacent to selected bond pads and forming joints between the selected bond pads and corresponding terminals of a carrier substrate.

Again, Beilstein does not expressly or inherently disclose a semiconductor device with bond pads adjacent an edge thereof. Nor does Beilstein disclose, either expressly or inherently, conductive bumps that are located adjacent to selected bond pads or that form joints between selected bond pads and their corresponding terminals of a carrier substrate.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(b), amended claim 9 is allowable over Beilstein.

Each of claims 10-12 is allowable, among other reasons, as depending from claim 9, which is allowable.

Independent claim 13, as amended and presented herein, recites a chip-on-board assembly that includes, among other things, a semiconductor device with bond pads located adjacent an edge of a surface thereof and arranged substantially in-line and electrically conductive joints configured to be disposed directly between and to establish communication between selected bond pads and corresponding terminals of a substrate.

By way of contrast with amended claim 13, Beilstein lacks any express or inherent disclosure of a semiconductor device with bond pads adjacent an edge of a surface thereof substantially arranged in-line or of a chip-on-board assembly including such a semiconductor device and electrically conductive joints directly between selected bond pads of the semiconductor device and corresponding terminals of a substrate. Rather, in Beilstein, a transfer metal 15 contacts a bond pad of a semiconductor device 13 and extends to an externally exposed electrical contact 27 of a module including a plurality of adjacent semiconductor devices 13. The electrical contact 27 of the module is, in turn, electrically connected to a corresponding contact 53 of a connection structure 41 by way of a conductive bump 29. Thus, it is respectfully submitted that none of the transfer metal 15, the conductive bump 29, or the transfer metal 15, electrical contact 27, and conductive bump 29 disclosed in Beilstein amounts to an electrically conductive joint that is located directly between the bond pad of the semiconductor device 13 and the contact 53 of the connection structure 41.

Therefore, under 35 U.S.C. § 102(b), amended independent claim 13 is allowable over Beilstein.

Claims 14-18 are also allowable, among other reasons, as depending either directly or indirectly from claim 13, which is allowable.

Additionally, independent claim 19, as amended and presented herein, is allowable over Beilstein as Beilstein lacks express or inherent disclosure of a computer that includes a semiconductor device comprising a "plurality of bond pads disposed on a surface of said semiconductor die proximate an edge thereof in a substantially in-line arrangement, each of said plurality of bond pads communicating with one of [a] plurality of circuit traces; and conductive bumps in communication with selected bond pads, said conductive bumps each configured to form a joint between one of said selected bond pads and a corresponding terminal of a substrate when said semiconductor device is positioned substantially vertical relative to said substrate." As stated above, Beilstein does not teach that bond pads are located adjacent to the edges of the semiconductor devices 13 disclosed therein. Moreover, in Beilstein, the conductive bumps 29 are located external to a multi-chip module that includes a plurality of stacked semiconductor devices 13 rather than forming a conductive joint between a bond pad and a corresponding contact 53 of the connection structure 41.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 102(b), amended independent claim 19 is allowable over Beilstein.

Claims 20-24 are each allowable, among other reasons, as depending either directly or indirectly from claim 19, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(b) rejections of claims 1-6 and 8-24 be withdrawn.

VI. Double Patenting Rejections

Claims 1-24 were rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 1-21 of prior U.S. Patent No. 6,140,696 for statutory-type double patenting.

With respect to double patenting rejections based on 35 U.S.C. § 101, M.P.E.P. § 804 provides:

> A reliable test for double patenting under 35 U.S.C. 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding

> claim in the patent [or related pending patent application]. *In re Vogel,* 422 F.2d 438, 164 USPQ 619 (CCPA 1970). Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting would not exist.

It is respectfully submitted that several embodiments of the claimed invention exist that fall within the scope of the presently claimed invention but not the cited patent. As the identical subject matter is not defined by the claimed invention of the present application and the claimed invention of United States Patent 6,140,696 (hereinafter "the '696 Patent"), no statutory double patenting exists.

Claim 1 has apparently been rejected as recited subject matter identical in scope to the subject matter recited in claim 1 of the '696 Patent.

While claim 1 of the above-referenced application recites a semiconductor device having a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof and arranged substantially in-line, claim 1 of the '696 Patent does not.

Therefore, presently amended independent claim 1 of the application is not subject matter identical in scope to the subject matter recited in claim 1 of the `696 Patent under 35 U.S.C. § 101.

Claims 2-6 and 8 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 7 has been canceled without prejudice or disclaimer, rendering the rejection thereof moot.

Independent claim 9 was apparent rejected as recited subject matter that is identical in scope to the subject matter of claim 8 of the '696 Patent.

While claim 9 recites a semiconductor device having a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof and arranged substantially in-line, claim 8 of the '696 Patent does not.

Therefore, presently amended independent claim 9 of the application is claiming a different invention than claim 8 of the `696 Patent under 35 U.S.C. § 101.

Each of claims 10-12 is allowable, among other reasons, as depending from claim 9, which is allowable.

The Office apparently rejected independent claim 13 on the basis that it recites subject matter which is identical in scope to the subject matter recited in independent claim 11 of the '696 Patent. While presently amended independent claim 13 of the above-referenced application recites a "semiconductor device having a plurality of bond pads on a surface thereof, each of said plurality of bond pads being located adjacent an edge of said surface and arranged substantially in-line", claim 11 of the '696 Patent does not.

Due to this clear difference in scope, it is respectfully submitted that claim 13 of the above-referenced application is allowable under 35 U.S.C. § 101 over claim 11 of the `696 Patent.

Claims 14-18 are each allowable, among other reasons, as depending either directly or indirectly from claim 13, which is allowable.

Independent claim 19 apparently stands rejected under 35 U.S.C. § 101 for reciting subject matter of a scope identical to that recited in claim 17 of the '696 Patent.

While the computer the presently amended independent claim 19 of the present application recites "a semiconductor die with a plurality of circuit traces and a plurality of bond pads disposed on a surface of said semiconductor die proximate an edge thereof in a substantially in-line arrangement", claim 17 of the '696 Patent does not.

Therefore, it is respectfully submitted that claim 19 is allowable under 35 U.S.C. § 101 over claims 17 of the `696 Patent.

Claims 20-24 are each allowable, among other reasons, as depending either directly or indirectly from claim 19, which is allowable.

For these reasons, it is respectfully requested that the 35 U.S.C. § 101 double patenting rejections of claims 1-6 and 8-24 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 1-6 and 8-24 is allowable. An early indication of the allowability of each of these claims is respectfully solicited, as is an indication that the case has been passed for issuance. If any issues preventing the allowance of any of claims 1-6 and 8-24 remain that might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned.

Respectfully submitted,

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BGP/sls:djp

Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Amended) A vertical surface mount semiconductor device, comprising:

a semiconductor device[;] having a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof and arranged substantially in-line[;] and having a plurality of conductive bumps disposed adjacent selected bond pads, each of said conductive bumps configured to form a conductive joint between at least one of said selected bond pads and a corresponding terminal of a substrate upon positioning said semiconductor device substantially vertically relative to said substrate.

2. (Amended) The vertical surface mount semiconductor device of claim 1, wherein a conductive [bum] bump is disposed adjacent each of said plurality of bond pads.

9. (Amended) A vertical surface mount semiconductor device, comprising:

a semiconductor device[;] having a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof and arranged substantially in-line, selected bond pads of said plurality of bond pads having conductive bumps adjacent thereto, said conductive bumps configured to form a [joints] joint between said selected bond pads and corresponding terminals of a carrier substrate upon substantially perpendicular orientation of said semiconductor device on said carrier substrate; and

a support member, at least a portion of which is disposed proximate said edge of said semiconductor device.

13. (Amended) A chip-on-board assembly, comprising:

a substrate with a plurality of terminals;

a semiconductor device configured to be positioned substantially perpendicularly relative to said substrate, said semiconductor device having a plurality of bond pads on a surface thereof, each of said plurality of bond pads being located adjacent an edge of said surface and arranged substantially in-line; and

electrically conductive joints configured to be disposed directly between and to establish communication between selected bond pads and corresponding terminals.

15. (Amended) The chip-on-board assembly of claim 13, further comprising a support member in contact with at least one of said semiconductor device and said [carrier] substrate.

19. (Amended) A computer including a vertically mountable semiconductor device, the semiconductor device comprising:

a semiconductor die with a plurality of circuit traces[;] and a plurality of bond pads disposed on a surface of said semiconductor die proximate an edge thereof in a substantially in-line arrangement, each of said plurality of bond pads communicating with one of said plurality of circuit traces; and

conductive bumps in communication with selected bond pads, said conductive bumps each configured to form a joint between one of said selected bond pads and a corresponding terminal of a substrate when said semiconductor device is positioned substantially perpendicularly relative to said substrate.